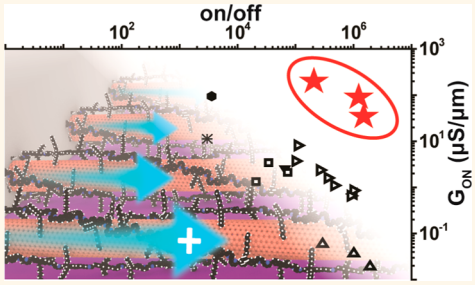
Polyfluorene-Sorted, Carbon Nanotube Array Field-Effect Transistors with Increased Current Density and High On/Off Ratio

Gerald J. Brady,[†] Yongho Joo,[†] Meng-Yin Wu,[‡] Matthew J. Shea,[†] Padma Gopalan,[†] and Michael S. Arnold*[,†]

[†]Department of Materials Science and Engineering and [‡]Department of Electrical and Computer Engineering, University of Wisconsin—Madison, Madison, Wisconsin 53706, United States

ABSTRACT Challenges in eliminating metallic from semiconducting single-walled carbon nanotubes (SWCNTs) and in controlling their alignment have limited the development of high-performance SWCNT-based field-effect transistors (FETs). We recently pioneered an approach for depositing aligned arrays of ultra-high-purity semiconducting SWCNTs, isolated using polyfluorene derivatives, called dose-controlled floating evaporative self-assembly. Here, we tailor FETs fabricated from these arrays to achieve on-conductance (G_{on}) per width and an on—off ratio (G_{on}/G_{off}) of 261 μS/μm and 2 $\times$ 10^5, respectively, for a channel length (L_{ch}) of 240 nm and 116 μS/μm and 1 $\times$ 10^6, respectively, for an L_{ch} of 1 μm. We demonstrate 1400$\times$ greater G_{on}/G_{off} than SWCNT FETs fabricated by other methods, at comparable G_{on} per width of ~250 μS/μm and 30—100$\times$ greater G_{on} per width at comparable G_{on}/G_{off} of 10^5—10^7. The average G_{on} per tube reaches 5.7 $\pm$ 1.4 μS at a packing density of 35 tubes/μm for L_{ch} in the range 160—240 nm, limited by contact resistance. These gains highlight the promise of using ultra-high-purity semiconducting SWCNTs with controlled alignment for next-generation semiconductor electronics.



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Single-walled carbon nanotubes (SWCNTs) have been widely recognized as promising candidates for next-generation field-effect transistors (FETs). The electronic properties of individual SWCNTs have been studied extensively in the diffuse (>1000 nm) and ballistic (<100 nm) charge transport regimes, revealing exceptional field-effect mobility[1] as high as 80 000 $cm^2/V/s$ and ballistic quantum conductance,[2] respectively. In FETs with a channel length (L_{ch}) shorter than 10 nm, like those planned for future integrated circuits, semiconducting SWCNTs are expected to outperform silicon, allowing for 2$\times$ the current density[3,4] with 2—3$\times$ lower power consumption.[5,6] In order to realize these gains in next-generation integrated circuits, it will be necessary to build FETs not from individual SWCNTs but aligned and tightly packed arrays of them.[7] However, thus far, it has been difficult to fully exploit the exceptional properties of individual SWCNTs in arrays because of materials challenges in the alignment and placement of SWCNTs, as well as in the removal of metallic SWCNTs.

The approaches that have been developed to create aligned SWCNT array FETs can be divided into two categories: (1) the direct growth of aligned SWCNTs *via* chemical vapor deposition and (2) their post-synthetic sorting and assembly. Progress has been made in improving directly grown SWCNT arrays by selectively heating[8] and burning[9—11] and thereby removing metallic SWCNTs and also in increasing the SWCNT density *via* iterative growth and transfer approaches.[12—14] Likewise, a number of post-synthetic sorting methods have been developed to separate metallic and semiconducting SWCNTs[15—19] and then to align them in arrays.[20—27] These advances have made it possible to increase the conductance (G_{on}) per width and conductance modulation (G_{on}/G_{off}) of both types of SWCNT FETs.[28—33] Nonetheless, current state-of-the-art array FETs still substantially underperform what should be realistically possible. It has especially been

* Address correspondence to msarnold@wisc.edu.

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difficult to simultaneously achieve high G_{on} per width and G_{on}/G_{off} in the same FET. This difficulty likely arises from residual metallic SWCNTs and organizational disorder, which can decrease both G_{on} and G_{on}/G_{off}.

Recently, we discovered a promising route toward overcoming these challenges. We pioneered an approach for depositing aligned arrays of highly purified semiconducting SWCNTs, isolated using polyfluorene derivatives, called dose-controlled, floating evaporative self-assembly (FESA).[34] In the initial screening of FETs fabricated from these arrays, we reported G_{on} per width of 61 μS/μm with a G_{on}/G_{off} of $\sim 10^5$ for FETs with L_{ch} = 400 nm and a packing density of 45 tubes/μm.[35] Here, we tailor FETs fabricated from these arrays to increase G_{on} per width by more aggressively scaling L_{ch}, improving the gate-coupling efficiency and improving the contact resistance and SWCNT processing parameters. Next, we more extensively evaluate the performance parameters of the SWCNT arrays using a Y function method to estimate the intrinsic channel conductance of the SWCNT FETs as a function of L_{ch}. Finally, we implement realistic models for the channel–gate capacitance that include disorder in the arrays to determine charge transport mobility in the percolating, long-channel regime (when L_{ch} is greater than the average SWCNT length and the aligned SWCNTs must percolate to span the channel) and to estimate a lower bound for the mobility in the direct, short-channel regime (when L_{ch} is less than the average SWCNT length and most of the SWCNTs directly span the channel).

RESULTS AND DISCUSSION

To fabricate FETs, we start with heterogeneous SWCNT soot grown by the arc discharge method. Ultra-high-purity semiconducting SWCNTs with diameters between 1.3 and 1.8 nm are extracted using the selective polymer poly[(9,9-dioctylfluorenyl-2,7-diyl)-*alt*-*co*-(6,6′-[2,2′-bipyridine])] (PFO-BPy) in toluene, adapting the procedures of Mistry *et al.* and our previous work.[36,37] The individual SWCNTs have a log-normal length distribution with an average length of 580 nm (Figure S1a,b). The purity and quality of the SWCNT material are verified *via* absorbance before alignment and FET fabrication in Figure S2a.

The SWCNTs are deposited as aligned arrays on HMDS/SiO_2/Si substrates *via* dose-controlled FESA at a packing density (ρ) of 28–49 tubes/μm.[34] Schematics of the FET architecture are shown in Figures 1a,b. Pd source and drain electrodes with a contact length (L_c) of 1.2 μm, a SiO_2 back-gate dielectric, and a heavily doped Si back-gate electrode are used. The channel width (W_{ch}) is 3.8 μm (about 104–185 SWCNTs), and L_{ch} is varied from 160 to 3070 nm. Experimental methods are further detailed below. Electron and atomic force micrographs (Figures 1c and S3) show that the SWCNTs are well aligned, with their long axis extending from source to drain.

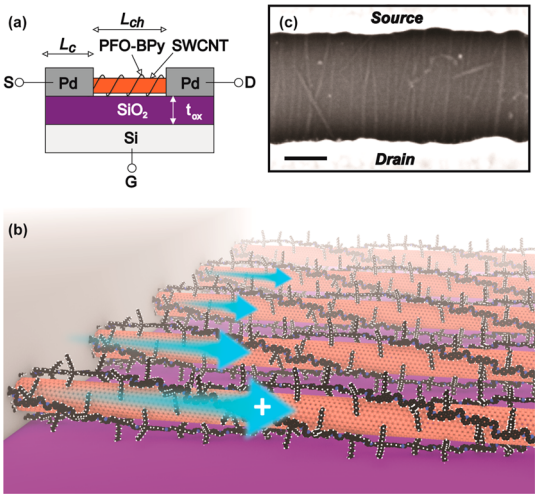

Figure 1. (a) Schematic of SWCNT FET architecture (not to scale). (b) Schematic of PFO-BPy-wrapped SWCNT arrays. (c) Top-down scanning electron micrograph of SWCNTs spanning Pd electrodes of a 240 nm L_{ch} SWCNT FET (scale bar = 100 nm).

In the initial screening of FETs fabricated from these arrays, G_{on} per width was limited to about 60 μS/μm for L_{ch} = 400 nm.[35] Here, we make several changes to increase G_{on} per tube and thus G_{on} per width. Namely, (1) we optimize the procedures by which excess polymer residues are removed from the aligned SWCNT arrays. In our initial work, we used short ultraviolet ozone radiation to reduce polymer residues. However, here we show that this treatment is detrimental, decreasing G_{on} per tube (Figure S4a). We instead use more extensive solvent rinsing and thermal annealing to reduce polymer residues (Figure S4b). (2) We decrease the total sonication time of the SWCNT solution from 31 min to 6 min (Figure S2b). (3) We decrease the SiO_2 gate oxide thickness from 90 nm to 15 nm to improve the capacitive coupling to the SWCNT array (Figure S5). We summarize the results in Figure S6 and demonstrate a 6-fold improvement in G_{on} per tube compared to the initial screening.

We examine three metrics to compare the properties of the optimized devices with the current state of the art: G_{on} per width, G_{on}/G_{off}, and G_{on} per tube as a function of packing density. The mean and standard deviation of G_{on} per width and G_{on}/G_{off} of the optimized FETs for L_{ch} = 160–240 nm, 1 μm, and 3 μm are compared to the current state of the art in Figure 2a.[8,11,24,38–45] G_{on} per width of the optimized FETs is increased by a factor of 6, on average, at constant G_{on}/G_{off}, compared to our initial screening (Table 1). The device-to-device variability in G_{on} per width of 20% for direct transport devices is typical for SWCNT array FETs.[46] When counting the exact number of SWCNTs that span the channel in each device, the variability in G_{on} per tube is a similar ~25% (see below).[33] Thus, other factors must be contributing to the variability in G_{on}. Overall, these FETs demonstrate

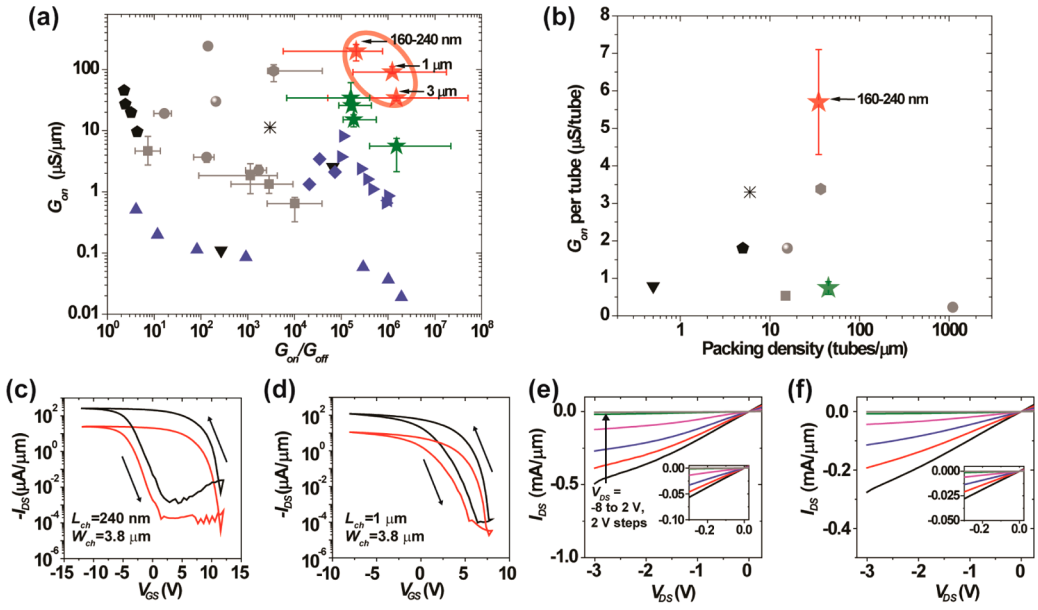

Figure 2. (a) G_{on} per width *versus* G_{on}/G_{off} literature comparison: Aligned CVD (black): pentagon,[39] down-triangles,[8] asterisk.[11] Postsynthetic random (blue): up-triangles,[44] left-triangle,[42] right-triangles,[43] diamonds.[40] Postsynthetic aligned (gray): squares,[38] circles,[24] hexagon,[45] sphere.[41] This work: optimized SWCNTs (red stars), initial screening (green stars).[35] (b) G_{on} per tube *versus* packing density for aligned SWCNT FETs presented in (a). (c) Transfer characteristics at $V_{DS} = -1$ V (black) and -0.1 V (red) for a champion SWCNT FET ($L_{ch} = 240$ nm and $W_{ch} = 3.8$ μm). (d) Transfer characteristics at $V_{DS} = -1$ V (black) and -0.1 V (red) for a champion SWCNT FET ($L_{ch} = 1070$ nm and $W_{ch} = 3.8$ μm). (e) Output characteristics of the device in (c) with V_{GS} swept from -8 V (black) to 2 V (gray) in 2 V increments. (f) Output characteristics of the device in (d).

TABLE 1. Comparison of Optimized SWCNT FET-Extracted Parameters at Various L_{ch}

L_{ch} (nm)	G_{on} per width (μS/μm)	log(G_{on}/G_{off})	G_{on} per tube (μS/tube)	μ (cm^2/V/s)
160−240	197 ± 38	5.13 ± 0.67	5.7 ± 1.4	
1070	95 ± 10	6.1 ± 0.74	2.4 ± 0.3	183 ± 18
3070	34 ± 3	6.2 ± 1.22	0.94 ± 0.15	179 ± 10
initial screening[35] (400 nm)	37 ± 9	4.9 ± 0.7	0.74 ± 0.16	

1400× greater G_{on}/G_{off} than SWCNT FETs made *via* other methods, at comparable G_{on} per width of ~250 μS/μm,[24] and 30−100× greater G_{on} per width, at comparable G_{on}/G_{off}[43] of 10^5−10^7 (Figure 2a).

The average G_{on} per tube for devices with L_{ch} = 160−240 nm is 5.7 ± 1.4 μS/tube at a packing density of 35 ± 6 tubes/μm. For comparison in Figure 2b, in previous array FETs, G_{on} per tube has been limited to less than 3.4 μS/tube. The G_{on} per tube reported here does not seem to be affected by internanotube screening effects because the G_{on} per tube in the aligned SWCNT FETs is equivalent to that measured in isolated SWCNT FETs fabricated from dilute spin-cast films. The product of the high G_{on} per tube and high packing density achieved here enables the high G_{on} per width.

The current−voltage characteristics of champion devices are shown in Figure 2c−f for FETs with L_{ch} of 240 and 1070 nm. Hysteresis is present, which is expected for back-gated SWCNT FETs measured in ambient.[8,47,48] The magnitude of the hysteresis may be affected by solvent or polymer wrapper residues and will be the focus of future studies. At an L_{ch} of 240 nm, G_{on} per width and G_{on}/G_{off} are 261 μS/μm and 2×10^5, respectively. The current output is 7.2 μA/tube at $V_{DS} = -1.0$ V. At an L_{ch} of 1070 nm, G_{on} per width and G_{on}/G_{off} are 120 μS/μm and 1×10^6, respectively. Although L_{ch} is about 4 times longer in the latter FET compared with the former, the conductance only decreases 2-fold, suggesting that contact resistance ($2R_c$) somewhat limits transport in the short L_{ch} regime.

Next, we analyze each device using a Y function method (YFM) to quantify $2R_c$.[49] Contact resistance at the electrode−SWCNT interface may arise from residues on the SWCNT surfaces following deposition that are not fully removed *via* postdeposition processing. These residues may originate from the polymer wrappers used to sort and disperse the SWCNTs or from solvents or polymers used during device fabrication. Short SWCNT−metal contact length may also lead to contact resistance.[50] Even though the length of our contacts is 1.2 μm, the latter is important because the average SWCNT length is only 580 nm. YFM is commonly used to extract device parameters for Si MOSFETs and was recently adapted for SWCNT FETs to

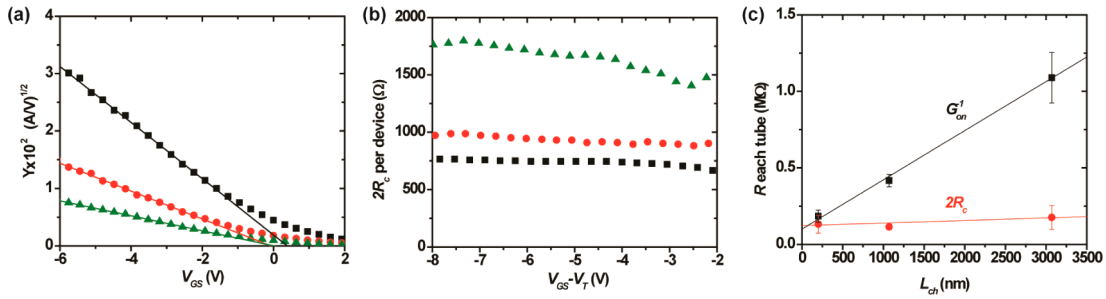

Figure 3. (a) YFM fits for representative FETs with L_{ch} = 200 nm (black squares), 1070 nm (red circles), and 3070 nm (green triangles). (b) $2R_c$ fit for the same devices in (a). (c) Measured G_{on}^{-1} (black squares) and $2R_c$ calculated by YFM (red circles) for the FETs presented in Figure 2a at various channel lengths (160−240 nm = 11 devices, 1070 nm = 4 devices, 3070 nm = 3 devices). Error bars denote one standard deviation.

measure $2R_c$.[51,52] To perform YFM analysis, the output current and transconductance are measured in the linear regime of the $I_{DS}-V_{GS}$ transfer curve at gate biases ranging from 1.2 to 8.0 V less than the threshold voltage (V_T). The Y function is plotted for three representative devices in Figure 3a with L_{ch} of 200, 1070, and 3070 nm following the relationship

$$Y = \frac{I_{DS}}{g_m^{1/2}} = (g_{ch}V_{DS})^{1/2}(V_{GS} - V_T) \qquad (1)$$

where $g_{ch} = \mu(W/L)C_{ox}$ is the $2R_c$-independent transconductance and is extracted from the slope of the linear region of the *Y versus* V_{GS} plot (Figure 3a).[49] The g_{ch} is further used below to calculate channel mobility based on YFM calculation. The threshold voltage (V_T) is determined from the *x*-axis intercept and is further used to calculate $2R_c$ according to

$$2R_c = \frac{V_{DS}}{I_{DS}} - \frac{V_{DS}}{g_{ch}(V_{GS} - V_T)} \qquad (2)$$

The extracted $2R_c$ of the three devices characterized in Figure 3a is analyzed as a function of V_{GS} in Figure 3b, demonstrating minimal V_{GS} dependence. $2R_c$ is averaged over a range of V_{GS} in the linear regime of Figure 3a. The mean and standard deviation of $2R_c$ on a single tube basis for all 18 devices are 136 and 60 kΩ, respectively. The minimum and maximum $2R_c$ are 66 and 260 kΩ, respectively. The large variability in $2R_c$ is separately confirmed using an L_{ch}-dependent transmission line method (TLM) to analyze the contact resistance of neighboring devices. The $2R_c$ determined *via* TLM similarly varies from 64 to 225 kΩ on a single tube basis (Figure S7a,b). The variation in $2R_c$ can potentially be attributed to residues or adsorbates that are not uniform on the substrate or to irregularities in the SWCNT packing arrangement that vary from device to device. The $2R_c$ variability is largely responsible for the device-to-device variability in G_{on} mentioned previously for L_{ch} = 160−240 nm.

We next compare $2R_c$ to the on-state device resistance (G_{on}^{-1}) on a single tube basis in Figure 3c. G_{on}^{-1} increases with increasing L_{ch}, while $2R_c$ remains fairly constant. At L_{ch} of 3070 nm, the SWCNTs percolate to span the FET channel, and G_{on}^{-1} and $2R_c$ are 1.1 ± 0.17 MΩ and 176 ± 78 kΩ, respectively, where the error bars denote device-to-device variability. The contact resistance contributes 8−21% of the total device resistance. At an L_{ch} of 160−240 nm, most of the SWCNTs directly span the channel, and G_{on}^{-1} and $2R_c$ are 185 ± 39 kΩ and 132 ± 57 kΩ, respectively, which are comparable to each other. In this direct transport regime, the devices are $2R_c$ limited and the contact resistance may roughly contribute anywhere from 50% to nearly 100% of the total on-state device resistance. The value of $2R_c$ is larger than the ∼10 kΩ that should ultimately be possible according to single SWCNT measurements.[50] However, the $2R_c$ of our champion devices (∼70 kΩ) is comparable to the lowest $2R_c$ that has been reported in CVD-grown aligned array FETs.[53,54] The $2R_c$ of solution-processed aligned array FETs has typically been much larger; for example, Cao *et al.* report a $2R_c$ of 6 MΩ.[24] The relatively low $2R_c$ is one reason that we achieve a high G_{on} per tube.

Next, the charge transport mobility, μ, is quantified in the percolating, long-channel regime, and a lower bound for μ is estimated in the direct, short-channel regime. The gate−channel capacitance per area (C_{array}) is evaluated in two ways. In the first approach, a regular array approximation is used where

$$C_{array} = \frac{\rho}{\left[C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_r}\ln\left(\frac{\sinh(2\pi t_{ox}\rho)}{\pi r\rho}\right)\right]} \qquad (3)$$

and $C_Q = 4 \times 10^{-10}$ F/m is the quantum capacitance, ε_0 is the relative permittivity of free space, $\varepsilon_r = (3.9 + 1)/2$ is the dielectric constant of the SiO_2/air interface, t_{ox} = 15 nm is the oxide thickness, r = 0.7 nm is the average radius of the SWCNT, and ρ is the linear SWCNT packing density. The array equation approach is valid assuming that the inter-SWCNT spacing exceeds the dielectric thickness,[39] which is true on average for the devices presented here. However, this approximation may not properly account for irregularities and disorder in the packing arrangement.

In the second approach, we calculate C_{array} *via* finite element (FE) modeling using COMSOL (COMSOL, Inc.,

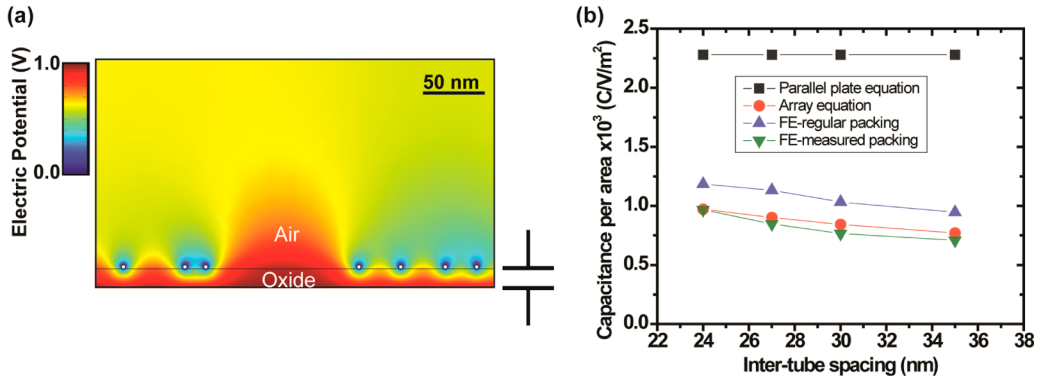

Figure 4. (a) Modeled electrostatic potential map of a measured SWCNT FET cross-section in COMSOL. The thickness of the oxide is 15 nm, with an average intertube spacing of 35 nm. The figure shows a 500 nm selected region of the 3.8 μm wide FET. (b) Summary of the gate−channel capacitance calculated for parallel plate equation (black squares), array equation (red circles), FE-regular packing (blue up-triangles), and FE-measured packing (green down-triangles).

Burlington, MA, USA) and considering disorder in SWCNT−SWCNT spacing. Disorder is quantified by measuring the position of each SWCNT in each FET *via* electron microscopy, across a cross-section extending along the center of the entire width of each channel (Figures 4a and S8). C_Q is then added in series with the capacitance calculated from the FE modeling according to

$$C_{array} = [C_Q{}^{-1} + C_{FE}{}^{-1}]^{-1} \quad (4)$$

A summary of the calculated gate−channel capacitances for various models and intertube spacing is presented in Figure 4b. The calculated capacitance for the measured packing arrangement is about 6% smaller than that determined from the array equation approximation and is used to determine the mobility at V_{DS} = −0.1 V according to

$$\mu = \frac{L_{ch} g_{ch}}{C_{array} W_{ch}} \quad (5)$$

At L_{ch} = 3070 nm in the percolating, long-channel regime, in which G_{on} is dominated by intra-SWCNT and SWCNT−SWCNT resistance, μ is 179 ± 10 cm^2/V/s, where the mean and standard deviation are calculated for the three devices measured. μ is similar at L_{ch} = 1070 nm. At L_{ch} = 160−240 nm in the direct, short-channel regime, charge transport is still expected to be diffusive. Studies of transport by Cao *et al.* of solution-processed SWCNTs have shown that transport is diffusive even at L_{ch} as small as 150 nm.[52] The YFM analysis of μ in the short-channel regime is less accurate because the contact resistance constitutes at least 50% of the on-state resistance. Therefore, to minimize the uncertainty, we analyze only a subset of devices with the smallest $2R_c$. The calculated μ ranges from 320 to 410 cm^2/V/s (Figure S9). The μ determined in both the short- and long-channel regimes *via* TLM analysis is similar (Figure S9). The increase in μ for L_{ch} < 300 nm likely arises because most of the SWCNTs directly span the channel, eliminating SWCNT−SWCNT resistance. It should be noted that the μ determined in the direct regime is likely a lower bound for the actual μ because YFM and TLM analyses underestimate μ when $2R_c$ varies from SWCNT to SWCNT within one FET and $2R_c$ and $G_{on}{}^{-1}$ are similar. The large variation of $2R_c$ from FET to FET suggests that $2R_c$ may vary within a single FET, as well. More extensive characterization of transport in the direct regime will be the focus of future study.

Regardless of whether μ is 320 to 410 cm^2/V/s or larger, the on-conductance of aggressively scaled sub-50 nm channels will almost certainly be limited by contact resistance, even if the contact resistance is substantially reduced. Thus, in order to increase on-conductance, future research should focus less on increasing mobility and more on decreasing contact resistance. Compared to CVD SWCNTs, the benefit of solution-processed SWCNTs is that it may be possible to achieve higher packing densities by circumventing the burn-out processes needed to eliminate metallic SWCNTs in CVD arrays. Thus, if contact resistance is optimized, the G_{on} per width should ultimately be higher for solution-processed SWCNTs, with the potential to outperform Si MOSFETs.

The fact that the mobility is still high, 180 cm^2/V/s, at long channel lengths indicates that the SWCNT−SWCNT coupling is excellent in the FESA-deposited SWCNT arrays, making them promising for more coarsely patterned FETs with >1 μm long channels. The alignment of the SWCNTs likely leads to substantially larger tube−tube overlap in comparison to the typical cross-junction overlap observed in percolating random networks. The mobility in the long-channel regime exceeds the ~100 cm^2/V/s that can be achieved using state-of-the-art inorganic amorphous semiconductors such as indium gallium zinc oxide.[55]

A final consideration is the semiconducting purity of the SWCNTs, which is evaluated by measuring G_{on}/G_{off} of the direct transport FETs and counting the number of tubes spanning each FET *via* SEM images. All of the SWCNT FETs measured have a G_{on}/G_{off} of >5 × 10^3 with

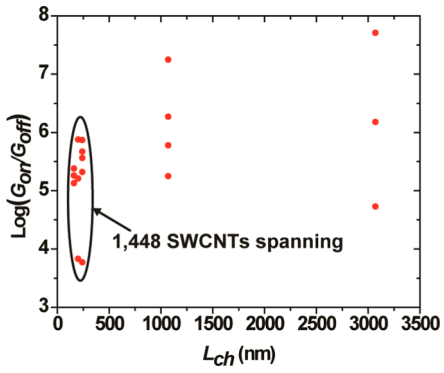

Figure 5. Log of on−off ratio for 18 devices with 11 devices measured at L_{ch} < 240 nm, four devices measured at L_{ch} = 1070 nm, and three devices measured at L_{ch} = 3070 nm. W_{ch} of all devices is 3.8 μm with similar packing density of about 40 tubes/μm.

most FETs having a G_{on}/G_{off} of $\geq 10^5$ (Figure 5), where a G_{on}/G_{off} of less than 10^2 indicates the presence of a metallic SWCNT. These data include more than 1448 SWCNTs measured in FETs with an L_{ch} of $\leq$240 nm, which directly span the channel, indicating that the metallic SWCNT impurity concentration is below one part per 1448. When our previous work is taken into consideration (4071 semiconducting tubes measured), we measure a metallic SWCNT impurity concentration of less than one part per 5519. The decrease of G_{on}/G_{off} with decreasing L_{ch} can potentially be explained by irregularities in the packing arrangements within the FET channels. It is clear from the AFM image in Figure S3c that some tubes cross and overlap, which indicates that there are regions along the length of the tubes that are not in intimate contact with the SiO_2 dielectric. When L_{ch} is short, some SWCNTs could potentially span the FET channel without ever making contact with the underlying gate dielectric. These noncontacting SWCNTs will be more poorly capacitively coupled to the gate, possibly preventing their complete turn-off. Implementation of a top gate dielectric will be the focus of future work, as it may lead to more uniform gating of the noncontacting SWCNTs.

CONCLUSIONS

We achieve 1400× greater G_{on}/G_{off} than the previous state of the art, at a comparable G_{on} per width of ~250 μS/μm. Likewise, we achieve 30−100× greater G_{on} per width than the previous state of the art, at a comparable G_{on}/G_{off} of 10^5-10^7. The excellent performance of the SWCNT FETs varying from L_{ch} much shorter to much longer than individual SWCNTs is attributed to the high semiconducting purity, degree of alignment, and packing density of the SWCNTs in the channel. The G_{on} per tube reaches 5.7 ± 1.4 μS and is limited by $2R_c$ on the order of 100 kΩ. Mobility is 179 ± 10 $cm^2/V/s$ at L_{ch} of 3 μm. These results show that substantially higher G_{on} per tube and per width should be possible by engineering the contacts and reducing the $2R_c$ and its variability. These gains highlight the promise of using ultra-high-purity solution-processed semiconducting SWCNTs with controlled alignment for next-generation semiconductor logic, high-frequency linear amplifiers, sensors, and flexible and stretchable electronics.

METHODS

Preparation of Arc Discharge@PFO-BPy Solutions. Large-diameter, semiconducting enriched SWCNTs are extracted from arc discharge carbon nanotube powder (Nanolab Inc., Waltham, MA, USA). A 1:1 weight ratio of 2 mg/mL of arc discharge soot and PFO-BPy (American Dye Source, Quebec, Canada, 48 K MW) is dispersed in 50 mL of toluene using a horn tip sonicator (Fisher Scientific, Sonic Dismembrator 500) at 64 W power. The sonication time of the initial dispersion is 30 min for SWCNTs prepared in the initial screening and in the surface treatment screening. Initial sonication time is decreased to 5 min after the surface treatment screening. Following the initial dispersion, the SWCNT solution is centrifuged (Thermo Scientific, Sorvall WX, swing bucket rotor, TH-641) at 300000*g* for 10 min to remove undispersed materials. The upper 90% of the supernatant is collected and centrifuged for an additional 1 h at 300000*g*. The upper 90% of the supernatant is collected, a 1 mL sample is collected for absorption analysis (see Supporting Information), and the rest is distilled to remove the toluene solvent. The gel-like PFO-BPy SWCNT mixture remaining after distillation is dispersed in tetrahydrofuran (THF). The solution is then centrifuged and dispersed with bath sonication four times in THF to rinse off as much excess PFO-BPy as possible. The final solution is prepared for floating evaporative self-assembly film deposition by horn-tip sonication of the rinsed SWCNT pellet in chloroform for a total of 1 min. The solution is diluted to a final concentration of 10 μg/mL prior to floating evaporative self-assembly film deposition and 0.5 μg/mL to prepare spin-cast films.

Preparation of Aligned SWCNT Films. During FESA, a receiving substrate is withdrawn from a water trough with control over position and velocity. A thin layer of "ink" (*i.e.*, PFO-BPy-wrapped semiconducting nanotubes in water-immiscible chloroform) is "floated" on the water surface. Here, we deliver ink to the trough surface in discrete "doses" (~2 μL droplets). Each droplet spreads until it reaches the substrate, after which a well-defined band of aligned nanotubes is deposited. The band extends across the entire substrate and grows in width as the substrate is withdrawn, until the ink layer is consumed due to evaporation.

SWCNT Surface Treatment Procedure. After depositing the aligned nanotube arrays and defining the channel region with electron-beam lithography (see below), the substrates are rinsed in an acetone bath at 120 °C for 5 min followed immediately by a 120 °C toluene rinse for 5 min and finally a 30 s rinse in isopropyl alcohol. Next the films are annealed in a tube furnace with a 99.999% pure 95% Ar:5% H_2 atmosphere at a temperature of 300 °C for 30 min.

SWCNT FET Fabrication. Prior to surface treatment electron-beam lithography is used to define a stripe width of ~4 μm, followed by an oxygen plasma etch that removes SWCNTs and material surrounding the FET channel. A second electron-beam step is used to define the source−drain electrodes, which are arranged side-by-side in an array, with different L_{ch}, along the same SWCNT stripe. Thermal deposition of palladium (40 nm) is used to create top contacts to the SWCNTs. Prior to measurement the SWCNT FETs are annealed at 200 °C in a tube furnace with an Ar (99.999%) atmosphere for 1 h.

Imaging. SEM images are collected with an LEO-1530 field-emission scanning electron microscope. Surface morphology and length distributions of the SWCNTs are imaged using a Nanoscope III Multimode atomic force microscope (Digital Instruments).

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Details on AFM length distribution and statistical analysis. Representative device SEM and AFM images. Optimization of surface treatment, sonication time, and gate oxide thickness. Transmission line measurement (TLM) and field-effect mobility calculation using TLM results. Finite-element modeling of channel–gate capacitance for various SWCNT packing arrangements. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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